ActaEnergetica
POWER ENGINEERING QUARTERLY

Design Structure of Compound Semiconductor Devices and Its Applications

Gudni Johannesson
PhD(Eng), Orkustofnun, The Icelandic National Energy Authority, Reykjavik, Iceland

Nazzal Salem
Department of Engineering, Zarqa University, Jordan

Keywords
Compound Semiconductor, Devices, MOSFET, electronics

Abstract
Due to their high carrier mobility, III-V compound semiconductors have begun to garner substantial interest as silicon-based electronics near their scaling limit for performance and chip density. The mobility advantages of III-V compounds are widely acknowledged, however this oversimplifies the detrimental impact of inevitable threading dislocations, which may seriously confine the utilization of these materials in nanometer-scale circuits. In this article, we give a hypothetical model that makes sense of how charged disengagements in quantum-bound III-V semiconductor metal oxide field impact semiconductors diminish transporter portability (MOSFETs). In light of the discoveries, we reach the determination that Fermi level sticking in the channel should be eliminated to deliver transporters with high infusion speeds for III-V compound MOSFETs to perform better compared to silicon MOSFETs.

Received by the editor: 22.03.2022
Received in revised form: 05.06.2022
Accepted: 25.06.2022

1. INTRODUCTION

Semiconductor devices are the foundation of practically all electrical and optoelectronic applications. In the electronics sector, silicon integrated circuits (ICs) incorporating a variety of advanced logic devices are prevalent [1]. High electron portability semiconductors, heterojunction bi-polar semiconductors, and integrated circuits are instances of business electronic devices based on III-V compound semiconductor substrates. Light emanating diodes and multi-quantum-well lasers are instances of economically available optoelectronic devices in III-V semiconductors. Arrays of infrared diodes and indicators are made for military and modern business sectors utilizing Hg1 xCdx Te or identical bandgap II-VI semiconductors. The field of silicon nanoelectronics, in which SijSiGejSi02 structures are utilized to build single electron metal-oxide-semiconductor semiconductors with nano-scale gate lengths, is a new development in semiconductor devices. The presentation of these devices is fundamentally subject to the fabrication process' honesty as far as layered exactness, interfacial response control, and part material virtue. While electrical estimations on the devices can give roundabout data on these material properties, portraying them requires direct data from different surface scientific techniques. Every strategy has unmistakable abilities in the investigation of primary highlights in the upper 1-2 f.!m of the surface where the devices and circuits are placed. Subsequently, a significant number of the troubles experienced in the improvement of semiconductor devices are adequately confounded to require the use of numerous techniques in tandem.

A. Compound semiconductor materials, devices and application

(1) Focus on optoelectronic materials, devices, and applications, such as semiconductor quantum dot lasers, infrared quantum cascade lasers, shortwave infrared photodetector applications in the aerospace industry, gas detection, etc.

(2) Epitaxial material for millimeter and submillimeter waves in the microwave: Focus on the materials utilized in ultra fast microelectronics, for example, the materials utilized in solid microwave integrated circuits, high electron portability semiconductors, heterojunction bipolar semiconductors, and thunderous burrowing devices, among others.

(3) Silicon-based III-V integration includes the growth of low dislocation density III-V compound semiconductor materials on silicon using the IMF method, the room-temperature growth of InAs quantum dot lasers by the growth of GaAs on Germanium, and the growth of the strained Ge film on a different III-V virtual substrate, among other applications.

(4) Research on new dilute bismuth infrared materials includes the growth of these materials on GaAs, InP, and GaSb substrates, a focus on the materials' structures and optical characteristics, and the creation of new dilute bismuth optoelectronic devices.

B. Compound Semiconductors

- Elemental semiconductors and compound semiconductors

The rapid development of electronics over the latter half of the 20th century significantly altered our way of life and civilization. The integrated circuit (IC), whose primary component is silicon, is unquestionably the key player in this advancement (Si). Element semiconductors, which are made up of a single element, are Si and Ge combined. Ge served as a warm-up act for Si as the first transistor material.

Compound semiconductors, then again, are semiconductors that are made by the ionic holding of different kinds of semiconductors. Ionic bond-shaped materials normally become protectors because of their intense electrostatic fascination. Due to their feeble electrostatic fondness to specific blends of anions and cations, they can sporadically change into semiconductors. Compound semiconductors and devices have been made and sold in a wide assortment up until this point. These compound semiconductors are sorted by the gathering number of the constituent components in the occasional table (Table 1), like III-V, II-VI, or IV. The III-V compound semiconductors GaAs, InP, GaN, and AlN are notable. ZnSe, ZnS, CaTe and SiC, separately, are notable II-VI and IV semiconductors. For more than 50 years, Sumitomo Electric has been making a few kinds of compound semiconductor materials. For the buyer and correspondence showcases, the organization has been essentially conveying III-V compound semiconductors, for example, GaAs, InP, Hole substrates and epitaxial wafers (Photograph 1), and all the more as of late, GaN substrates for Blu-beam plates' blue-violet lasers.

Table 1. Major compound semiconductor element periodic table

II	**III**	**IV**	**V**	**VI**
	B	C	N	O
	Al	Si	P	S
Zn	Ga	Ge	As	Se
Cd	In	Sn	Sb	Te

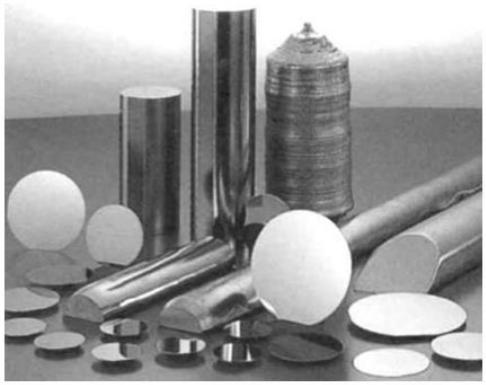


Figure .1: Compound semiconductors such as GaAs and InP

C. Electron Devices

Compound semiconductors are necessary for the production of nearly all of the photonic devices mentioned in Section 3. On the other hand, Si, not compound semiconductors, is used to make the majority of commercial electron devices, such as

transistors. However, higher performance electron devices with features like low noise or high frequency operation can be made utilising compound semiconductors. GaAs or InP can operate at high speeds and frequencies, while SiC or GaN can operate at high voltages and low losses. This section describes several compound semiconductor electron devices that have been created so far.

- High frequency electron device

Because of its higher electron portability contrasted with Si from the 1970s to 1990s, GaAs was an exceptionally encouraging material for the utilizations of rapid semiconductors or integrated circuits, and a few examination projects were completed worldwide. Because of the low point of interaction state thickness at Si/SiO2 interfaces, MOSFETs (metal-oxide-semiconductor field impact semiconductors), which utilize the electric channels created there, are a typical decision for Si electron devices. GaAs can't deliver excellent connection points with its oxide or dielectric materials like Si can. GaAs MOSFETs were not created accordingly. The creators utilized an assortment of assembling techniques to concentrate on GaAs MOS models. Despite the fact that it was feasible to fundamentally diminish the connection point state thickness by anodizing the saved aluminum on GaAs or utilizing a Ga-doped SiO2 layer to prevent Ga from diffusing into the SiO2 film(49)- (51), business GaAs MOSFETs couldn't be made.

GaAs MESFETs (metal-semiconductor field effect transistors), which utilised Schottky barrier junction as gate electrodes, were used as element transistors in integrated circuits (ICs) because GaAs MOSFETs could not be produced (54). GaAs ICs were anticipated to supplant Si ICs due to their high speed and low power dissipation qualities, however they were unable to reach the LSI market due to Si ICs' quick performance improvement. However, small size ICs are frequently employed as amplifiers and drivers for optical fibre communication systems as well as switching and amplifier ICs for wireless communication systems.

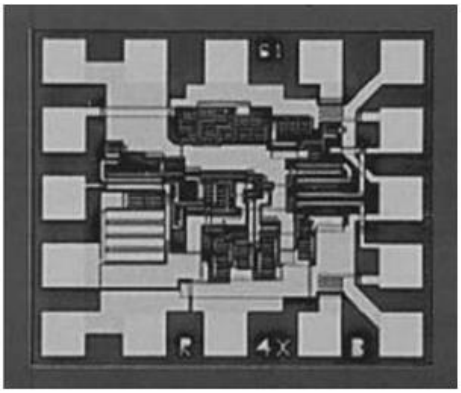


Figure.2: Photomicrograph of GaAs amplifier IC

2. LITERATURE REVIEW

Graphene Nanorippon FETs are another significant possible structure in semiconductor technology that was highlighted in ITRS (2011). Graphene, which is 100 times quicker than silicon, is one of the most crucial materials for nanoelectronics in the future. Additionally, compared to carbon nanotubes, graphene material has an extraordinarily high carrier mobility. Carbon atoms that have undergone sp2 hybridization and are bound together in graphene have benzene ring configurations. Exfoliated graphene, with a mobility of 2,50,000 Cm2/Vs, gives the maximum mobility possible among all graphene materials. Back-gated graphene, a different kind, provides field effect mobility up to 10,000cm2 /Vs. The grapheme mobility with SiO2 provides electron mobility as 40,000 cm2/Vs at normal temperature. At ambient temperature, the mobility of such a device has been enhanced to 100,000 cm2/Vs when boron nitride is employed as the substrate for a graphene channel. Extremely high carrier mobility is provided by epitaxial graphene, which is 15000 cm2/Vs at ambient temperature and 2,50,000 cm2/Vs at liquid helium temperature, respectively (Xinran Wang et al. 2008 & Palacios et al. 2010). Because the gate dielectric might damage the electrical characteristics of graphene, the top-gated graphene channel transistor offers lower field effect mobilities than others. Buffer layers are utilised between graphene and high K materials to prevent deterioration. The top gated graphene, which uses Al2O3 as the gate dielectric, provides the maximum field effect mobility of 23,600Cm2/Vs. The RF application of the graphene Nanorippon FETs in VLSI technology (Grassi et al. 2008)

The next generation nanoscale structure has been discussed by ITRS (2013), and it includes spin FET and spin MOSFET transistors. Variable current

drivability, which may be regulated by the magnetization arrangement of ferromagnetic electrodes, is one of the key properties of a spin transistor. This function is ideal for extremely energy-efficient and low power architectures and is very helpful. There are two different types of spin transistors: spin FETs and spin MOSFETs. Controlling the transistor output through spin or magnetization is a key characteristic of the spin transistor (Sugahara and Nitta 2010). Based on its source/drain structure and source/drain material—Ferromagnetic Metal (FM), Half Metallic Ferromagnetic (HMF), or Ferromagnetic Semiconductor—Spin MOSFETs can be categorised (FS). The ferromagnetic semiconductor material for the channel should be carefully chosen to maximise the functionality of the spin MOSFET. The spin MOSFETs are appealing fundamental components for reconfigurable logic gates and non-volatile memory cells. 2003's (J. Schliemann et al.)

The basics of group III-V semiconductor MOSFETs were presented by Serge Oktyabrsky in 2010. Despite the fact that SOI MOSFETs have fewer short channel effects, these effects might result in poorer mobility, which reduces speed and increases delay. To alleviate the problems caused by silicon material, other greater mobility materials have gained relevance in semiconductor technology. One such option is the use of IIIV and germanium materials in modern semiconductor devices. In SOI MOSFET devices, the germanium and III-V compound materials are used as a channel material that can take the place of the traditional silicon channel material. Thus, binary, teranary, and quaternary group of elements such as gallium arsenide (GaAs), gallium nitride (GaN), indium phosphide (InP), and zinc sulphide can be used to create compound semiconductor materials (ZnS). As a result, high mobility III-V semiconductors and a high-k gate dielectric will be crucial components of nanoscale MOSFET technology in the future.

Lu Zhou (2018) has suggested that a III-V compound semiconductor material with a high surface density—more than 1013 C/m2—such as GaAs, InGaAs, GaSb, InP, InAs, or InSb, which causes Fermi level pinning and surface recombination to accelerate and worsens device performance. Sio2 layer on Si provides outstanding interfacial characteristics and strong thermal stability in conventional MOSFETs. While III-V semiconductor is used as the channel material in MOSFETs, its native oxides can cause undesirable surface defects because of its poor thermal stability. For optimal device performance, it is crucial to passivate the III-V surface. In semiconductor technology, several methods like chemical etching, ion sputtering, and controlled annealing are utilised to enhance the surface and interface quality.

3. METHOD

In this article, we offer a model for the transporter dispersing brought about by charged disengagements in III-V semiconductor MOSFETs that are quantum-restricted. We select Ino.53Ga,A7As as a channel material from the accessible Sick V materials on the grounds that InuaGao.47As is the most broadly involved Sick V divert material in field impact semiconductors as a result of its exceptionally negligible cross section confuse with silicon substrate and rather high electron portability. Two essential effects result from displacements situated lined up with the transporter travel heading. One is the consequence of the nuclear displacement of separations, which has a twisting potential. The impact is considerably lesser because of the separations' smaller scope of communication contrasted with the other, long-range dissipating instruments since the disfigurement potential they make is essentially nonpartisan (except for the piezoelectric coupling situation). Because of the charges being caught at disengagements, the subsequent impact is the Coulomb expected irritation. The significant impact results from the Coulomb cooperation among transporters and charged separations since it has an extensively more extensive territory than the deformity likely connection. Any Evil V compound semiconductor material with an overwhelming conduction valley at the gamma point and practically symmetric compelling masses, no matter what the bearing of transporter transport, can utilize the model. The model's semi-all inclusive relevance to all Evil V materials with separations can be accomplished by altering the materials properties that our model considers.

4. RESULT & DISCUSSION

Systems like balance molded channel field impact semiconductors (FinFETs), channel on-separator semiconductors, and quantum all around bound high electron versatility semiconductors are instances of quantum-confined (with discrete energy levels) MOSFETs (HEMT). Since we are managing the

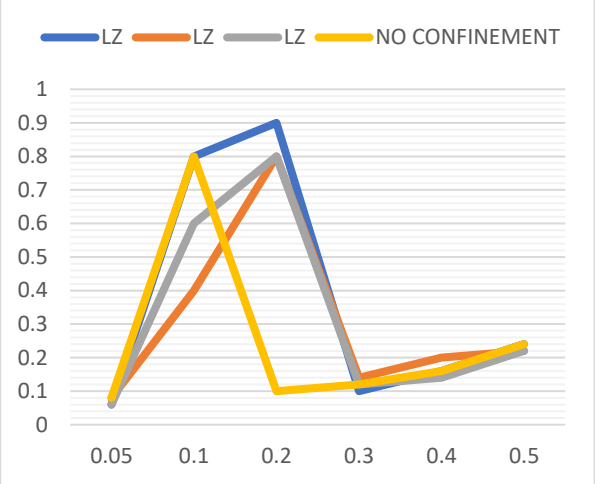
MOSFET on-express, the free transporter thickness is exclusively impacted by the substance capability of the channel transporters, which is controlled by the gate voltage, instead of by the impartiality prerequisite. Since stringing separations will generally arrange toward epitaxial advancement, we further accept in this examination that disengagements are typical to the Int 536a0A7As surface. In Fig. 1, the schematic of our model is shown. Ints3Gatxas FinFET transporter dissipating occasions are displayed in Figure 1 with a charged disengagement that is vertical to the top gate, near the channel's middle, totally charged, and screened by the free encompassing transporters.

The making of acceptor-like imperfection states by arsenide separations, which act as electron and opening recombination places or electron traps, is irrefutably factual. In this review, we propose that at a high electron synthetic expected comparative with the conduction band edge in the channel, these initially vacant acceptor-like snares are filled by one electron for each cross section length boundary (semiconductor on-state). In the on-state FinFET with quantum restriction in the channel width bearing, we initially decide the pace of transporter energy unwinding welcomed on by the Coulomb communication with charged separations (z-course). For the motivations behind this calculation, we expect to be that the episode (starting) electrons' wave-vector k is in the x-course (channel length heading). The dispersed (last) wave-vectors, then again, can contain components in both the x and z headings. We guess that main in the z-course — the bearing of the channel's width — do gate oxide hindrances compel waves; in the x-heading, the wavefunction is pretty much a free wave capability. Disregarded are the entrances of the electron wave capability into the gate oxide, which can be considered a genuine expansion in restriction width. Subsequently, the underlying and end wave capabilities can be depicted in the following manner.

$$\psi_i = \frac{1}{\sqrt{L_x L_z}} \sin(k_z z) e^{ik_x x} \qquad , \psi_f = \sqrt{\frac{2}{L_x L_z}} \sin(k_z z) e^{ik_x x} \ ,$$

The channel length and width are represented by the subscripts L and IL, the beginning wave-vector is represented by the subscript k, and the final wave-vectors in the x- and z-directions are represented by the subscripts kz and Itz. The quantized wave-vector kz can take on discrete values of not/I., n. =1, 2, 3, etc. The scattering caused by the dislocation line charges cannot modify the momentum in the line direction, hence the y components of the wave-vectors are not taken into account. This situation's scattering physics can therefore be thought of as a two-dimensional problem. 4. The dislocation scattering rate (Sa,$) can be stated as following from the transition rate relation of elastic scattering that results in Fermi's golden rule and screening effect that takes into consideration the Coulomb potential expression in the momentumspace.

ne(m^{-3})	LZ	LZ	LZ	NO CONFINEMENT
0.05	0.06	0.08	0.06	0.08
0.1	0.8	0.4	0.6	0.8
0.2	0.9	0.8	0.8	0.1
0.3	0.1	0.14	0.12	0.12
0.4	0.16	0.2	0.14	0.16
0.5	0.24	0.22	0.22	0.24



$$S_{dis}(k) = \sum_f \sum_i W_{f,i}(1 - \cos\theta_k) = \frac{4L_y N_{dis} e^4 m^*}{h^3 L_x L_z^2 (\varepsilon c)^2} \sum_{n_x} \lambda^4 \ (1 + \sqrt{1 - (n_2\pi/kL_z)^2}) \times (1 + 2k(k \pm \sqrt{k^2 - (n_z\pi/L_z)^2})\ \lambda^2)^{-2}$$

The progress rate from the I state to the f state for this situation is W1. m' is the powerful mass of electrons in the channel, 0 is the point between the underlying and last wave-vectors, Nth is the quantity of charged separations in the channel, E is the dielectric permittivity of the I The grid boundary

along thelno meta, 4, is "no c." The energy conservation relation determines the maximal number, n, which is a positive odd number including zero, as the direction of layer growth, and X, which is the Debye length.(= $(\varepsilon k_B T/e^2 n_e)^{1/2}$)We refer to changes in effective mass that depend on confinement length and come from non−parabolic band as

$$m^* \cong m^{*0}\sqrt{1+2\frac{h^2\pi^2}{L_z^2 m^* q}}$$

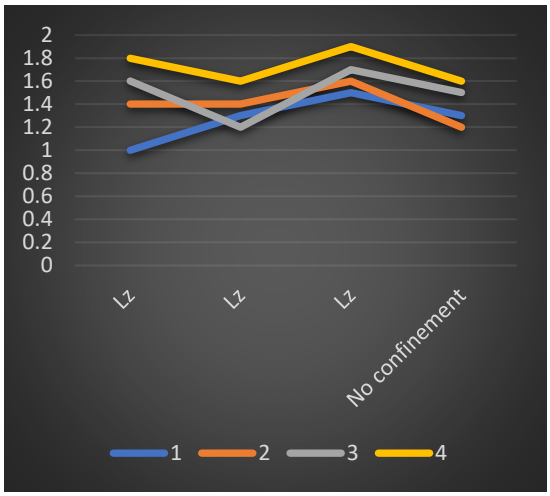
Here, nr°is the bulk effective mass in the Inc,,,Gat,,As r-valley (=0.041 nk,). In order to perform Fourier integration for the derivation of Eq. (2), we presupposed that the Debye length, which is normally —I nm, is shorter than the confinement length (L). The free electron density can be visualised as the sum of all potential energy levels below the Fermi energy and depends on the carrier's Fermienergy.

$$n_e = \frac{m^*}{\pi h^2 \beta L_z}\sum_{\varepsilon_i} \ln\left(1+e^{(E_F-\varepsilon_t)/k_B T}\right)$$

Here, e is the conduction band's 0' possible energy, quantized in the z-direction and below the Fermi energy (Es), and an is equal to 1/kBT. With In0.53Ga0A,As the channel material, the noticed free electron densities are shown in Fig. 2 as an element of the Fermi energy for different channel widths (1..). The Fermi energy and free transporter thickness have a roughly direct relationship, as anticipated by Eq. (4). Because of the developing absolute volume with expanding channel width, the figured electron volume thickness is contrarily relative to the channel width. As the channel width approaches limitlessness, as shown by the dabbed line in Fig. 2, the transporter thickness moves toward the best isotropic, endless three-layered transporter thickness (- 4/37r 2). There is a non-disappearing electric field in the channel despite the fact that the electric field in the channel is exceptionally negligible because of the low activity voltage for downscaled devices. The electrons' Fermi-Dirac appropriation not entirely set in stone by this electric field and the dissipating episodes. By using the unwinding time guess to settle Boltzmann's vehicle condition, which is upheld by the way that Coulomb dissipating is versatile, the circulation can be communicated concerning the electric field and dispersing time as follows.

$$f(k) = f_0(k) + \delta f(k)$$
$$= f_0(k) - \frac{e}{h}\tau_{dis}(k)\vec{E}.\nabla_k f_0(k)$$

Bulk silicon	Lz	Lz	Lz	No confinement
1×10^{25}	1.0	1.3	1.5	1.3
2 ×10^{25}	1.4	1.4	1.6	1.2
3 ×10^{25}	1.6	1.2	1.7	1.5
4 ×10^{25}	1.8	1.6	1.9	1.6



CONCLUSION

For charged separation scatterings in quantum-bound MOSFETs, we have made a hypothetical model. The Ints,GaLcAs channel framework was utilized to test the model, which was supposed to show fundamentally more noteworthy transporter portability than silicon in the separation free condition. For an extensive variety of Fermi energies (EF 03 eV), the anticipated separation versatility was even not exactly that of mass silicon. This revelation drives us to the determination that a nano-scale III-V compound semiconductor device loses its benefits over silicon assuming that it displays the undeniable disengagement that happens when it is made on a silicon wafer (s). Two essentials should be fulfilled for this issue to be addressed. For one's purposes, a high working voltage is important to increment transporter speeds, and for the other, an almost ideal match between the gate oxide and Sick V channel material is important to eliminate Fermi level sticking. The last option, notwithstanding, is as yet an issue, while the previous is obliged by the spilling power issue. In transporter bound devices with all the dispersing sources, for example, surface

unpleasantness dissipating, phonon dissipating, and interface trap dispersing, the determined portability values were contrasted and tentatively estimated compelling versatility values to appraise the disengagement dissipating impact. This examination drives us to the end that, in quantum-restricted, short channel MOSFETs, disengagement dissipating might be the dominating dispersing system. The semiconductor cell would breakdown because of this outrageous loss of the successful channel portability, at last prompting the disappointment of the whole rationale chip.

FUTURE WORK

(1) Explore the uses of compound semiconductor devices in infrared, gas detection, and other applications using an application-oriented perspective;

(2) Conduct thorough analysis and epitaxial material optimization for microwave, millimetre wave, and sub-millimeter wave applications in order to establish the basis for China's ultra-high-speed microelectronics technology;

(3) Conduct research on the innovative silicon/germanium-based optoelectronic devices for applications in silicon-based optoelectronics;

(4) Conduct research on the new dilute bismuth III-V materials and work to increase the global influence in the new III-V materials' fundamental studies.

REFERENCES

1. Y. Matsui, H. Hayashi, M. Takahashi, K. Kikuchi, and K. Yoshida, "(InAs)m(GaAs)n superlattices grown by molecular beam epitaxy," J. Crystal Growth, 71, p.280 (1985).
2. Y. Matsui, H. Hayashi, K. Kikuchi, and K. Yoshida, "(InAs)m(GaAs)n superlattices grown by Beam-separation MBE method," International Conference on Modulated Semiconductor Structures (1985).
3. Y. Matsui, H. Hayashi, and K. Yoshida, "Temperature dependence of electron mobility in (InAs)3(GaAs)1 superlattices," Appl. Phys. Lett., 48, p.21 (1986).
4. Y. Matsui, N. Nishiyama, H. Hayashi, K. Ono, and K. Yoshida, "InAsGaAs superlattices as a new semiconductor grown by beam separation MBE method," International Symposium on GaAs and Related Compounds, Inst. Phys. Conf. Ser., 91, p.179 (1987).
5. N. Nishiyama, H. Yano, S. Nakajima, and H. Hayashi, "(InAs)3(GaAs)1 superlattice channel field-effect transistor grown by molecular beam epitaxy," Appl. Phys. Lett., 55, p.894 (1989).
6. N. Nishiyama, H. Yano, S. Nakajima, and H. Hayashi, "InAs-GaAs superlattice/N-Al0.48In0.52As modulation-doped field effect transistor grown by molecular beam epitaxy," International Symposium on GaAs and Related Compounds (1989).
7. N. Nishiyama, H. Yano, S. Nakajima, and H. Hayashi, "n-AlInAs/ (InAs)3(GaAs)1 superlattice modulation-doped field effect transistor grown by molecular beam epitaxy," Electronics Letters, 26, p.885 (1990).
8. H. Kamei and H. Hayashi, "OMVPE growth of Ga1-xInxAs/InP (0.53⩽x⩽0.71) quantum wells with extremely narrow photoluminescence linewidths," Technical Digest of Indium Phosphide and Related Materials, p.389 (1991).
9. H. Kamei and H. Hayashi, "OMVPE growth of GaInAs/InP and GaInAs/GaInAsP quantum wells," J. Crystal Growth, p.567 (1991).
10. T. Katsuyama, I. Yoshida, and H. Hayashi, "Highly uniform GaInP and AlGaInP/GaInP QW structures grown by organometallic vapor phase epitaxy," International Symposium on GaAs and Related Compounds (1989).
11. H. Kamei, H. Hayashi, Y. Michitsuji, M. Takahashi, M. Maeda, and H. Okuda, "Uniform lasing characteristics of 1.3-μm multiple quantum-well Fabri-Perot laser diodes over 2-inch-daiameter wafer with excellent high temperature operation," Technical Digest of Optical Fiber Communication Conference, p.127 (1991).
12. K. Yoshida, K. Matsumoto, J. Fukui, T. Nakabayashi, A. Miki, M. Yoshimura, T. Iwasaki, G. Sasaki, and H. Hayashi, "Development of an Uncooled Coaxial DFB-LD Module for Analog Transmission," SEI Technical Review, 48, P.76 (1998).
13. H. Kamei, M. Yoshimura, H. Kobayashi, N. Tatoh, and H. Hayashi, "High-power operation of 1.48 μm GaInAsP/GaInAsP strained-layer multiple quantum well lasers," 1991 Technical Digest Series, 13, Optical Amplifiers and Their Applications, p.30 (1991).
14. H. Kamei, N. Tatoh, J. Shinkai, H. Hayashi, and M. Yoshimura, "Ultra-high output power of 1.48 μm GaInAsP/GaInAsP strainedlayer multiple quantum well laser diodes," International Conference on Optical Fiber Communication (1992).
15. N. Tatoh, H. Kamei, K. Tanida, J. Shinkai, M. Shigematsu, M. Nishimura, H. Hayashi, and K. Nawata, "High power, high reliability 1.48 μm strained-layer multiple quantum well laser and its

application to high performance Erbium-doped fiber amplifier," International Conference on Optical Fiber Communication (1993)